

Preface

The statement “it's a digital world” is a gross simplification of reality. There is no doubt that digital content in electronics design is growing geometrically with Moore's law. However, the addition of integrated analog functions, third-party IP, power management, and software is creating an exponentially-scaled verification problem. Furthermore, this scaling virtually guarantees that inconsistent verification approaches will introduce problems because every project involves multiple, often third-party, global project teams. The convergence of new functionality, exponentially-scaled verification, and distributed teams at advanced nodes such as 20 nm creates operational pressure as companies try to profitably meet the verification requirements of modern Systems on Chip (SoCs). Following the conventional engineering approach to address a huge system, industry-leading teams established a controlled, working base for their verification environment and then built upon that base. Those teams built and selected the Universal Verification Methodology (UVM) standard from Accellera as that base because it is architected to scale with the growing size of digital verification. As the UVM base expands, verification managers and team leaders are now asking “what's next?”

The answer to that question depends on the requirements that SoC verification adds on top of digital verification. An SoC that a team assembles from internal and 3rd-party hardware IP may be primarily digital, but it clearly needs to integrate verification IP (VIP) from multiple sources. If the commercial differentiation of the SoC depends on unique features, then mixed signal and low power are likely to be critical next steps. Verification capacity and the means to automate a comprehensive verification plan are the areas of focus when the SoC is so large and complex that it can only be implemented in the latest available node.

Of these requirements, VIP integration is the most common. Today, the UVM language standard is IEEE 1800 SystemVerilog, but many UVM users need to access VIP written in IEEE 1647 *e* or IEEE 1666 SystemC. Because many SystemVerilog verification teams would like to easily integrate VIP or models written in different languages, it is essential that the UVM is extended to support multi-language, interoperable verification environments. Doing so builds on the reuse inherent in the UVM and preserves the quality coded into the existing VIP.

Almost as pervasive as VIP for SoC integration are low-power and mixed-signal needs. Starting as a trend in the deep-submicron era and continuing through 20 nm and below, the drive toward further integration assures that nearly every SoC will have this extra complexity. For low-power design, the change becomes evident in the move from simple clock gating to power shutoff, voltage scaling, and other methods that frequently have multiple hardware and software controls. As a result, the handful of directed tests that once verified the power modes are no longer sufficient to assure proper power response in tens or hundreds of

thousands of sequences that verify the function of the SoC. A better approach is to make the base UVM environment power aware, thereby fusing functional and power verification. Similarly, the hardware function of the SoC itself is increasingly dependent on both analog and digital circuits, so mixed-signal verification needs to be added to this fused solution. Adding these extra capabilities to the verification task raises analog-specific questions about simulation speed, modeling abstraction, coverage, and assertions. While some standards in the mixed-signal space, including IEEE 1800 SV-DC (analog modeling for SystemVerilog), remain in-flight at the time this book was written, many of the capabilities to implement a working methodology do exist because project teams are fusing low-power, mixed-signal, and UVM functional verification for 20 nm designs today.

Scaling is third requirement. It is pervasive at 20 nm, but becomes evident in the increased complexity nearly every team deals with in each project. Verification engineers assembling the full SoC for verification are seeing turn-around time for big software-based verification runs slowing significantly as their projects grow. While hardware-based verification does not suffer the same effect, it appears to be out-of-reach technically for many teams. By creating a connection to the UVM for the testbench, hardware-based acceleration becomes a more attractive option for software-based verification teams. Of course, those teams can only reach the point of integrated SoC acceleration by standing on the shoulders of the block and subsystem verification work already completed. Teams know they can stand firmly on this quality base if they have followed a metric-driven verification methodology (MDV) that captures metrics at every stage and maps these metrics back to their verification plan.

Consumers may perceive that “it’s a digital world,” but these advanced verification topics speak to the magic that goes on under the hood of every SoC. As verification engineering managers and team leaders, we know that MDV, multi-language VIP, low-power, mixed-signal, and acceleration topics are converging at 20 nm and beyond; but we don’t want to create whole new methodologies for each one. The authors of this book realized this, and selected the Accellera UVM standard as the common base from which to offer solutions that leverage reuse and raise team-level productivity. That’s why we have written this book—not only for verification engineers familiar with the UVM and the benefits it brings to digital verification, but also for verification engineers who need to tackle these advanced tasks. Though the solutions in this book are not standardized, most of them are available through open-source code. For all of you, the material in this *Advanced Verification Topics* book is provided as a means to stay productive and profitable in the face of growing verification complexity.

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